CLAIMS

What is claimed is:

1. A method for insulating a lower layer of a semiconductor device from an upper layer of the semiconductor device comprising the sequential steps of:

(a) providing an interlayer dielectric on the lower layer;

(b) providing an antireflective coating (ARC) layer, at least a portion of the ARC layer being on the interlayer dielectric;

(c) providing a plurality of via holes in the interlayer dielectric and the ARC layer;

(d) filling the plurality of via holes with a conductive material; and

(e) removing the ARC layer while reducing subsequent undesirable charge gain and subsequent undesirable charge loss over the use of a chemical mechanical polish in removing the ARC layer.

2. The method of claim 1 wherein the ARC layer removing step (e) further includes the steps of:

(e1) removing the ARC layer using a plasma etch.

3. The method of claim 2 wherein the plasma etch further utilizes a CH_3F/O_2 chemistry or a CHF_3/O_2 chemistry.

4. The method of claim 1 wherein the conductive material used to fill the

plurality of via holes is W.

5. The method of claim 1 wherein the interlayer dielectric is BPTEOS.

6. The method of claim 1 wherein the lower layer includes a plurality of memory cells and is a first layer fabricated on the semiconductor device.

7. The method of claim 1 further comprising the step of:

(f) providing a chemical mechanical polish of the conductive material.

8. A semiconductor device including a lower layer and an upper layer, the semiconductor device comprising:

an interlayer dielectric between the lower layer and the upper layer, the interlayer dielectric having a plurality of via holes therein;

a plurality of contacts filling the plurality of via holes in the interlayer dielectric, the plurality of contacts including a conductive material;

wherein the plurality of via holes are formed in the interlayer dielectric using an antireflective coating (ARC) layer on the interlayer dielectric, the ARC layer being removed after formation of the plurality contacts such that subsequent undesirable charge gain and subsequent undesirable charge loss are reduced over the use of a chemical mechanical polish in removing the ARC layer.

9. The semiconductor device of claim 8 wherein the ARC is removed using a

plasma etch.

10. The semiconductor device of claim 9 wherein the plasma etch further utilizes a CH_3F/O_2 chemistry or a CHF_3/O_2 chemistry.

11. The semiconductor device of claim 8 wherein the conductive material used to fill the plurality of via holes is W.

12. The semiconductor device of claim 8 wherein the interlayer dielectric is BPTEOS.

13. The semiconductor device of claim 8 wherein the lower layer includes a plurality of memory cells and is a first layer fabricated on the semiconductor device.